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IN THE SPECIFICATION

Please amend the specification as follows:

At page 3, line 10:

The data access controller 30 ~~transfers a fourteen bit~~ receiving an external row address signal AD<0:13> transfers a fourteen bit signal to the first cell block 21 and the second cell block 22 at a data access operation, or transfers the fourteen bit row address signal A<0:12> to each of the two cell blocks 21 and 22 fixing a highest row address signal A <13> at the refresh operation.

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At page 8, line <sup>12</sup>~~18~~:

The first sense amplifier controller 560 is controlled by a first RAS control signal RASCTL0\_OUTPUT outputted from the first RAS controller 510 to generate a first sense amplifier control signal SACTL0\_OUTPUT. The first cell block 580 includes a plurality of memory cells. The first sense amplifier unit 590 is for amplifying data included in selected memory cells that are transferred through lines BLT0 and BLB0.

At page <sup>9</sup>~~10~~, line <sup>24</sup>~~7~~:

The second sense amplifier controller 660 is controlled by a second RAS control signal RASCTL1\_OUTPUT outputted from the second RAS controller 610 to generate a second sense amplifier control signal SACTL1\_OUTPUT. The second cell block 680 includes a plurality of memory cells. The second sense amplifier unit 690 is for amplifying data included in selected memory cells memory cells that are transferred through lines BLT1 and BLB1.

At page 10, line <sup>9</sup>~~17~~:

The first control unit 720 generates the first cell mat enable signal BAI for enabling the first cell mat 500 using a bank address signal BA. The second control unit 730 receives the first cell mat enable signal BAI and outputs the second cell mat enable signal BA8KI without delay at the data access operation; however, at the refresh operation, the second control unit 730 outputs

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the second cell mat enable signal BA8KI after delaying the first cell mat enable signal BAI for a predetermined time decided by a delay unit (tD) 740.

At page 13, line <sup>18</sup>~~29~~<sub>K</sub>:

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Referring to Fig. 4, the bank controller 700 outputs the first cell mat enable signal BAI and the second cell mat enable signal BA8KI at the same time during data access operation (this operation period is marked as 'X'); however, the bank controller 700 outputs the first cellm at enable signal BAI first, then, outputs the second cell mat enable signal BA8KI after the predetermined time tD at the refresh operation (this operation period is marked as 'Y'). Each operation period is determined by commands REF and ACT.